## REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-6 are presently active in this case; Claims 7-21 having been withdrawn from consideration, and Claim 1 having been amended by way of the present amendment.

In the outstanding Official Action, Claims 1-6 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogura et al (U.S. Pat. No. 6,255, 166), Pradeep et al (U.S. Pat. No. 6,228,713), and Jang et al (U.S. Pat. No. 5,786,262). Claims 2, 3, and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ogura et al, Pradeep et al, and Jang et al, and further in view of Reisinger (U.S. Pat. No. 6,137,718). Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al, Pradeep et al, Jang et al, and Reisinger, and further in view of Agarwal et al (U.S. Pat. No. 6,201,276). Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura et al and Pradeep et al, and Jang et al, and further in view of Fang (U.S. Pat. No. 6,023,085).

Regarding the 35 U.S.C. § 112, second paragraph, rejection to Claims 1-6, Claim 1 has been amended to more particularly point out that the charge storage layer in the first transistor exist only below a first gate electrode in an element region. Thus, it is respectfully submitted that the 35 U.S.C. § 112, second paragraph, rejection has been overcome.

The outstanding final Office Action rejected Claim 1 as being obvious over Ogura et al in view of Pradeep et al, and Jang et al which was newly cited in the outstanding final Office Action. The final Office Action acknowledges that Ogura et al do not show a first and second transistor isolated by a trench.[1] Furthermore, the final Office Action acknowledges that Ogura et al does not disclose the features set forth in Claim 1, concerning the first

transistor having the above charge storage layer and the second transistor isolated by a trench.[2]

Further, the final Office Action notes that Pradeep et al teach to isolate memory cells with trench isolations 24 in element isolation regions with the charge storage layer 14, and also notes that Jang et al teach to form a bottom insulating layer in a trench's inner surface 10 to provide better isolation.[3] The final Office Action therefore concludes that Claim 1 is obvious over those three references. However, Applicant respectfully submits that the asserted combination of Pradeep et al and Jang et al in the final Office Action will not produce the claimed invention.

According to Pradeep et al, as shown in Fig. 7A thereof, the floating gate 14 is formed below the top surface of the trench isolation (STI) insulating film 24, and the side surface 14A of the floating gate 14 contacts the side surface of the STI insulating film 24, directly. Meanwhile, Jang et al shows in Fig. 10 that a lining oxide film 14 is formed on the inner surface of the shallow trench 10 by the thermal annealing.

If the technique of Pradeep et al concerning the configuration including the floating gate 14 and the STI insulating film 24, and the technique of Jang et al regarding the lining oxide film 14 are combined, then the resultant configuration will be quite different from the features set forth in Claim 1. For example, performing the thermal annealing process set forth in Jang et al on the STI insulating film 24 of Pradeep et al to form the lining oxide film 14 of Jang et al will oxidize the side surface 14A of the floating gate 14 of Pradeep et al. Therefore, such a combination of Jang et al and Pradeep et al will form an oxide film on the side surface 14A of the floating gate 14 of Pradeep et al.

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[1] Office Action, page 3, lines 13-19.
[2] Id., page 3, lines 13-19.
[3] Id., page 3, line 20, to page 4, line 8.

As a result, a width of the floating gate 14 of Pradeepet al (i.e., the layer in Pradeep et al identified in the final Office Action as the charge storage layer) will be ***equal to or less than*** a width of an element region, because of the resulting width of the oxide film formed on the side surface 14A of the floating gate 14.

However, Claim 1 defines that a width of a charge storage layer corresponds to a width of an element region of the semicondcutor substrate and a thickness of a bottom insulating film. Thus, as shown illustratively in Applicant's Figure 11, the width of the charge stroarge layer 112 is wider than the width of the elemental region 101 underneath the bottom oxide layer 111. Yet, as shown above, the combination of the thermally oxidized oxide film 14 of Jang et al with the floating gate of Pradeepet al would produce a width of the floating gate ***equal to or less than*** a width of an element region. To otherwise restrict the teachings of Jang et al to a non-thermally oxidized oxide film 14 would be an example of the impermissible picking and choosing of selected features of Jang et al based on impermissible hindsight, and would make the asserted combination of Pradeep et al and Jang et al improper.

Therefore, neither Pradeep et al nor Jang et al individually nor when combined disclose the features set forth in Claim 1, i.e., that a width of a charge storage layer corresponds to a width of an element region of the semiconductor substrate and a thickness of a bottom insulating film.

Accordingly, Applicant respectfully submits that Claim 1 and the claims dependent therefrom are believed to patentably define over the applied prior art.

This amendment is submitted in accordance with 37 C.F.R. §1.116 which after final rejection permits entering of amendments canceling claims, complying with any requirement of form expressly set forth in a previous Office Action, or presenting rejected claims in better form for consideration on appeal. The present amendment clarifies Claim 1 to address the 35

U.S.C. § 112, second paragraph, rejection identified in the Office Action, and then sets forth reasons why the combination of Pradeep et al with newly cited Jang et al does not produce the claimed invention or is otherwise improper. No new matter has been added, and this amendment does not raise new issues requiring further consideration and/or search. It is therefore respectfully requested that the present amendment be entered under 37 C.F.R. §1.116.

Consequently, in view of the present amendment and in light of the above discussions, the outstanding grounds for rejection are believed to have been overcome. The application, as amended herewith, is believed to be in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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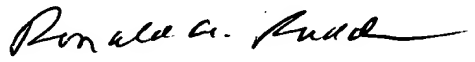

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